

# TRB Developments

Michael Traxler for the TRB Collaboration

2015-11-13

# Outline

## TRB Developments

Michael Traxler  
for the TRB  
Collaboration

TRB Platform

Experiences and  
Limits

Next Step:  
DiRICH

Summary

- 1 TRB Platform
- 2 Experiences and Limits
- 3 Next Step: DiRICH
- 4 Summary

# TRB: Features I

## TRB Developments

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## TRB Platform

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Summary

- Versatile and meanwhile technically **mature** platform for TDC measurements and digital readout
- consists of FPGA-firmware, DAQ- and calibration-software and hardware
- most important ingredient: the TRB team behind all of it for (necessary) support
- many channels (256) on one board and as cheap as possible
- leading edge time precision: 8-12ps RMS
- hitrates  $< 50\text{MHz}$  (burst)
- DAQ: 140MBytes/s via two 1GbE links

# TRB: Features II

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## TRB Platform

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Summary

## Hardware

- motivated to be independent from not easy to acquire ASICs from the community
  - based on FPGAs (TDC, DAQ, FEE-Discriminator) and other parts with a second source
  - We misuse digital FPGAs in the asynchronous and analogue domain



# TRB Platform: TRB3 module

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Summary



- 4 times high speed 208-pin connector for various AddONs
- Addons available:
  - 6 port Hubs
  - NIM/ECL-Input
  - ADC
  - standard 100mil pins
  - Padiwa-Adapter
  - etc.

# TRB Platform: Some Hardware II

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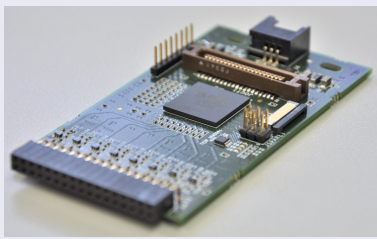
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Limits

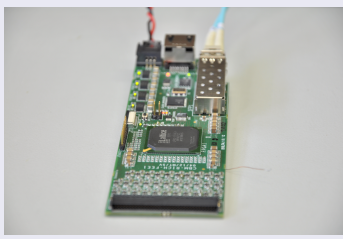
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Summary

Padiwa



CBM-TOF-FEE



- Padiwa used for CBM-RICH-beamtests
- Padiwa used for Panda-Barrel-DIRC-beamtests  
Summer 2015 at CERN
- CBM-TOF-FEE used for CBM-TOF beamtime  
November 2015 at CERN

# TRB Platform: Some Hardware III

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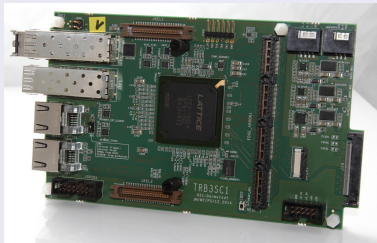
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Summary

TRBsc



TRB3sc Crate



- 1/4 of TRB3 on a single card
- fits in 19" standard crate system with FPGA-connectivity in backplane
- better DC/DC converters for better time precision
- higher DAQ speed

# New Features and Performance

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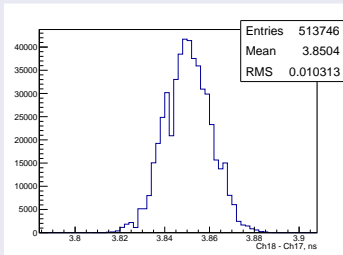
Experiences and  
Limits

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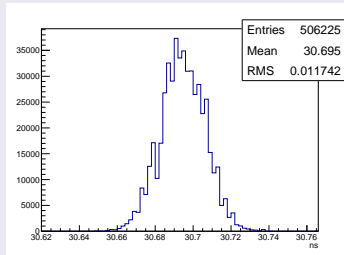
Summary

The TDC can now stretch the falling edge of a pulse and reuse the channel to measure the Time over Threshold of an input pulse. The performance is still good.

ToT: alternating channels



ToT: new stretcher



# Performance ToT with Stretcher

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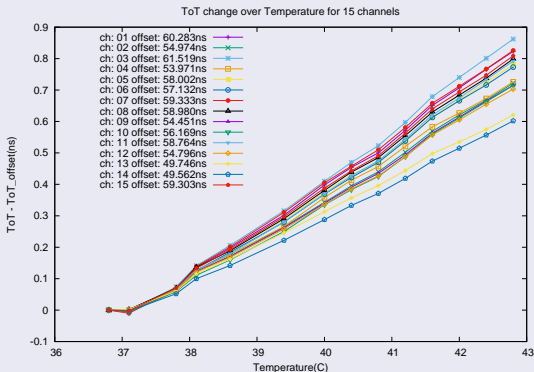
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Summary

## ToT vs. Temperature



The long (~35ns) signal propagation in the FPGA results in a strong temperature dependence of the ToT

# Performance ToT with Stretcher II

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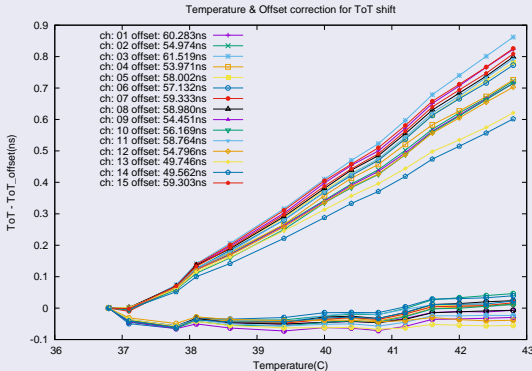
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## ToT vs. Temperature



This effect can be corrected later and suppressed to a 65ps shift for a 6K temperature shift.

# Plans for TDCs and Current Status

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Summary

- using higher clock frequencies for the TDC delay line register will result in shorter delay lines and (most likely) less resource usage
  - more channels can fit into one FPGA
- A 10 weeks large scale intense test at GSI for the upcoming CBM-TOF beamtime has been performed
  - more subtle bugs have been identified and have been removed
  - The famous "dying-channel" bug first encountered during the Barrel-DIRC-CERN beam time has been tracked, reproduced and is now removed.
  - High data rate DAQ-hangups don't occur anymore (actually a solid workaround)
  - We reached a state (since 6 weeks :-)) of **no** known bugs!

# Feature and Problem at the same Time

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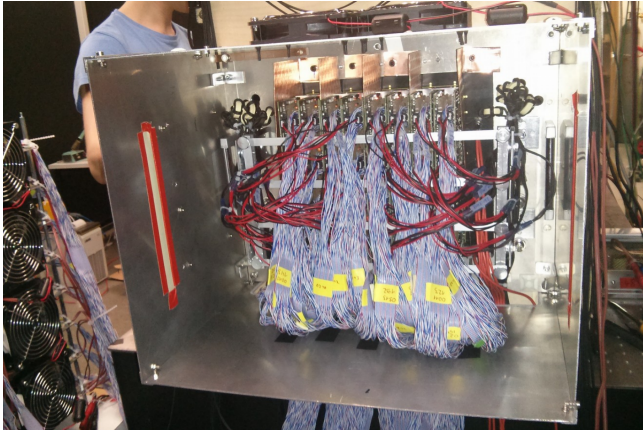
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- The TRB platform is a stable and flexible
- Flexibility has a (high) price
  - Cables everywhere!





# Effects of Cables

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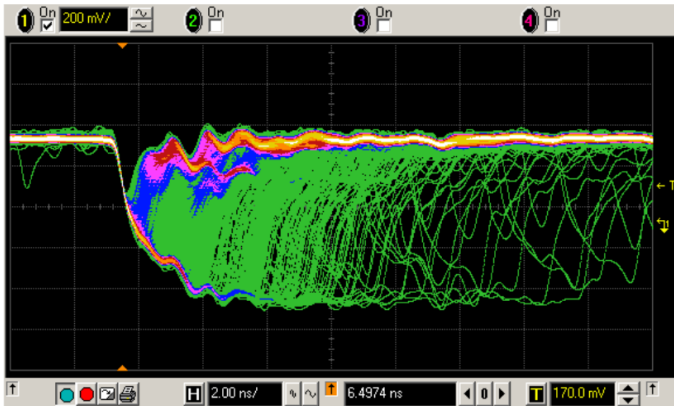
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Summary

- Mechanically this becomes a problem (densities)
  - Barrel-DIRC-beam-time clearly showed that this is more than a inconvenience
- Long cables damp the signal away



# Further Encountered Problems

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- The FEE is stable in the lab in small setups
- In a larger setup a high frequency feedback from the FEE to the MCP-PMTs and back to other channels of the FEE has been observed
- Result: high frequency oscillation forced the use of unreasonable high thresholds
- Only solution available: attenuate high frequency noise at the input of the 3GHz amplifiers
  - disadvantage: slower rise time of the signal + smaller amplitude
  - needs higher amplification and is more affected to lower frequency noise
- Net effect: degradation of timing performance from 30ps RMS to TBD ps RMS ( $<100$ ps RMS)

# Degradation of Measured Time Precision Due to Attenuation of Input Signal

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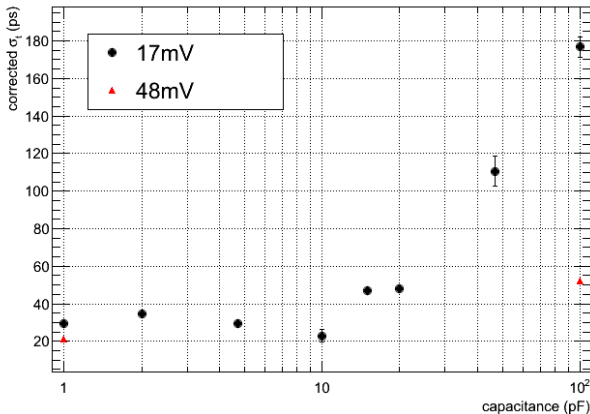
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PADIWA Input Capacitance Test



# Solution

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## Experiences and Limits

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Summary

- Rethink mechanics/cables/connectors
- Improve on noise to the input of the FEE
- Improve on noise immunity of FEE
- Work together in a larger team!
- Some pressure!

# RICH700 Project in HADES: to be finished in 2016

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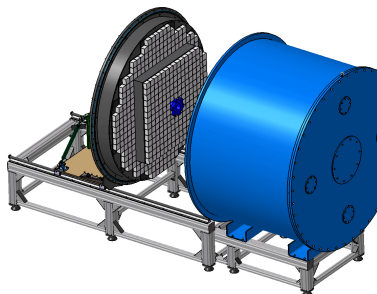
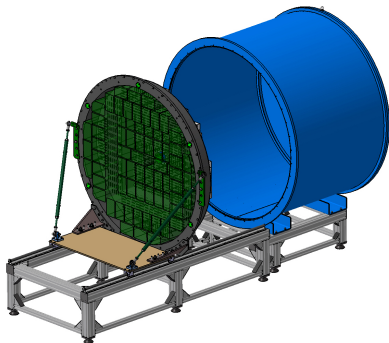
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Experiences and  
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Next Step:  
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Summary

- Exchange of the HADES RICH CsI photocathode with 420 MA-PMTs
- New FEE + Readout has to be developed
- Cooperation of CBM + HADES experiments



# HAL9000: Inspiration

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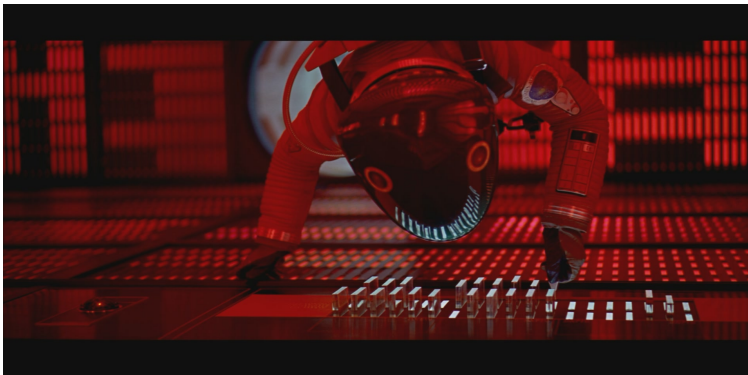
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Summary

- First you need some sort of epiphany :-)



# Backplane Granularity and Dimensions: Long and Tedious Optimization

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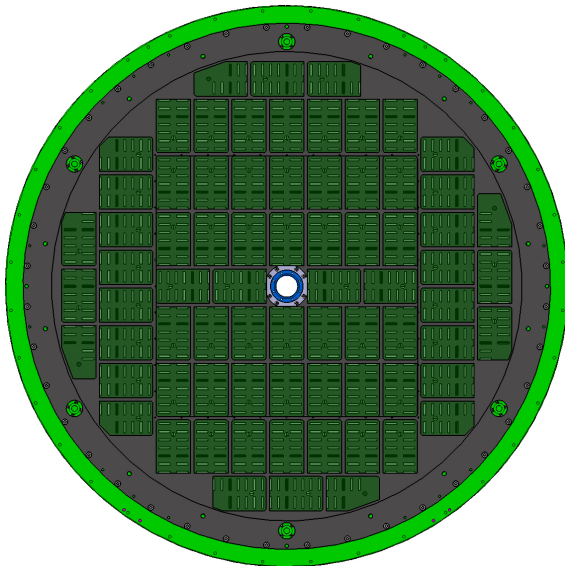
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# DiRCH concept

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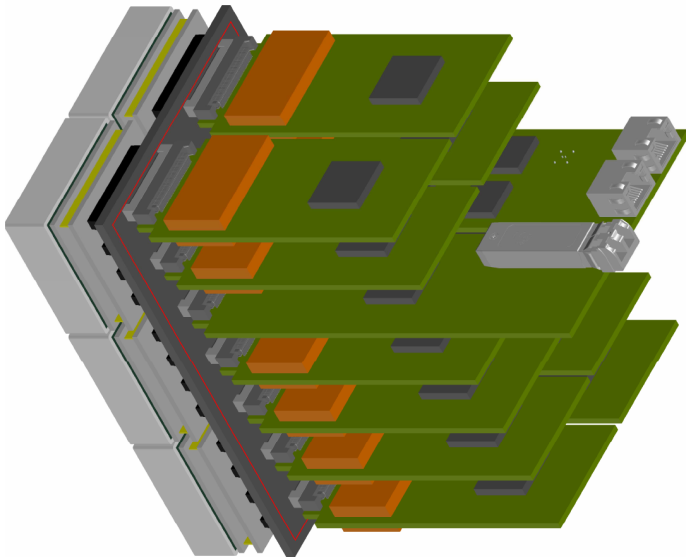
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# DiRICH Requirements and Design Consequences

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Summary

- FEE module for 32 channels
- Amplification, Discrimination, TDC + DAQ
- no cables
- analog input signals and digital output signals (serial transmission) over the same connector
- low power consumption
- only possible with newest FPGAs (price/performance) and most dense connectors

# DiRICH: Some New Ideas

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Summary

- galvanically isolate PMT from FEE with transformers
  - reduces issues with HV-Power-Supply GND connection
  - brand new  $2.2 \times 1.5 \text{ mm}^2$  transformer types available
- reduce bandwidth of amplifiers (transistor based compared to MMICs) to needed minimum
  - ASICs available for this task? PADI is a candidate.
- Status
  - schematics are done (mainly connectors)
- Challenges + Risk
  - PCB Layout: technically and **manpower**

# Summary

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## Next Step: DiRICH

## Summary

- TRB platform reached a mature state
- lessons have been learned
- next steps are customization for  
HADES/CBM-RICH and Barrel-DIRC projects
- far advanced state for HADES-RICH project
- large overlap for FEE and mutual benefit is large  
(tests, measurements, etc)
- not without risks!