TRB/DiRICH FEE Electronics and Readout System

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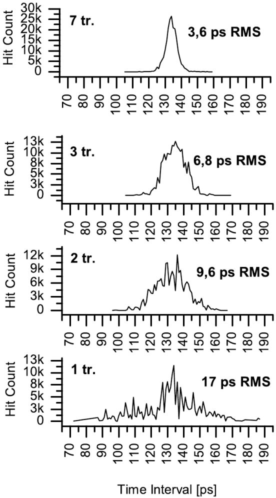
Outline

TRB: FPGA TDC

- FPGA TDCs can be very precise
- tradeoff between timing precision and resources
- FPGA TDCs are flexible
- implemented features can change (trigger, windows, scalers, etc.)
- new ideas pop up quite often (e.g. smart charge measurement, etc.)



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TRB: Features

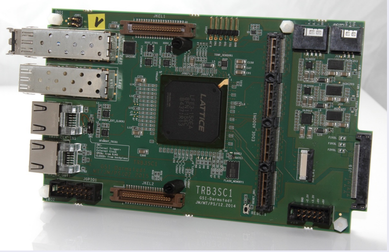
- Versatile and meanwhile technically mature platform for TDC measurements and digital readout
- consists of FPGA-firmware, DAQ- and calibration-software and hardware
- most important ingredient: the TRB team (a collaboration) behind all of it for the (necessary) support [trb.gsi.de]
- many channels (256 single edge, 192 with ToT and internal stretcher) on one board and as cheap as possible
- leading edge time precision: 8-12ps RMS
- hitrates: <50MHz (burst)
- DAQ: 140MBytes/s via two 1GbE links

TRB: Motivation and Future

- motivated to be independent from not easy to acquire ASICs from the community
- based on FPGAs (TDC, DAC, DAQ, FEE-Discriminator) and other parts with a second source
- We misuse digital FPGAs in the asynchronous and analog domain
- channel price "automatically" drops with new FPGA generations
  - we started 5 years ago with 170EUR/FPGA with 150k LUTs
  - now we are at 19.50EUR/FPGA for 85k LUTs
  - factor of 5 in performance/price increase (or larger)
- game-changer: FPGA/TDC/DAC/Discriminator are now not the price determining part of the system anymore!
- Enables the use of FPGAs everywhere in the Front-End

TRB Platform: Some Hardware

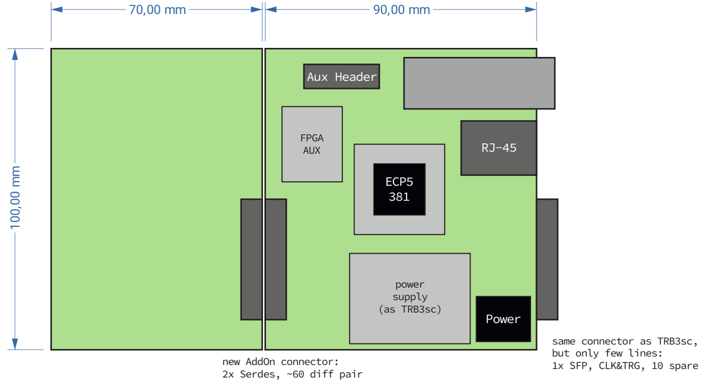
TRBsc



TRB3sc Crate

- 1/4 of TRB3 on a single card
- fits in 19" standard crate system with FPGA-connectivity in backplane
- better DC/DC converters for better time precision
- higher DAQ speed

TRB5sc: Planned Hardware



- used in TRB3sc crate
- standardized "backend": TDC (high or low precision)
- pluggable Front-End-Electronics: easy to develop!
- pioneering users: PANDA/HADES-Forward Tracker, PANDA-Straw-Tube Tracker

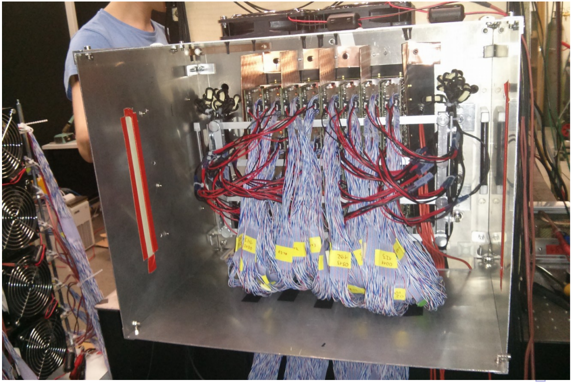
Experiences and Limits

What did we learn?

- TRB DAQ-Systems work very well and stable also for large systems
- FPGA-TDC working horse of the whole DAQ/FEE-system
- Padiwa-FEE works for many users very well
- but. . . .

Feature and Problem at the Same Time

- The TRB platform is a stable and flexible
- Flexibility has a (high) price
  - Cables everywhere!
- Mechanically this becomes a problem (densities)
- Long cables damp the signal: loss in efficiency

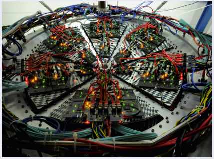


Solution

- Rethink mechanics/cables/connectors
- Improve on noise to the input of the FEE
- Improve on noise immunity of FEE
- Work together in a larger team!
- Add some pressure!

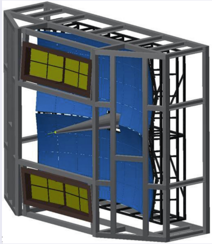
Team for a Total of ~100k channels

HADES-RICH



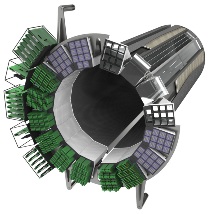
- 28k channels MA-PMT
- beamtime in Q4 of 2018

CBM-RICH



- 55k channels MA-PMT

PANDA-Barrel-DIRC



- 11k channels MCP-PMT
- smaller signals

TRB Collaboration

Team of ~8 developers (hard- and software)

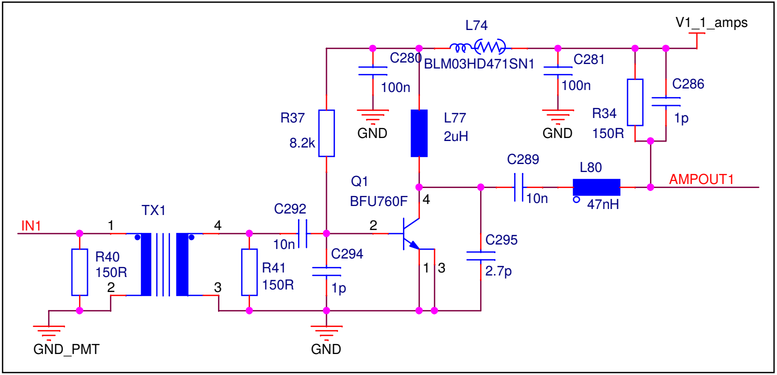
RICH700 Project in HADES: Electronics

- Talk of Vivek Patel: "The HADES RICH upgrade and CBM RICH concept"

DiRICH Requirements and Design Consequences

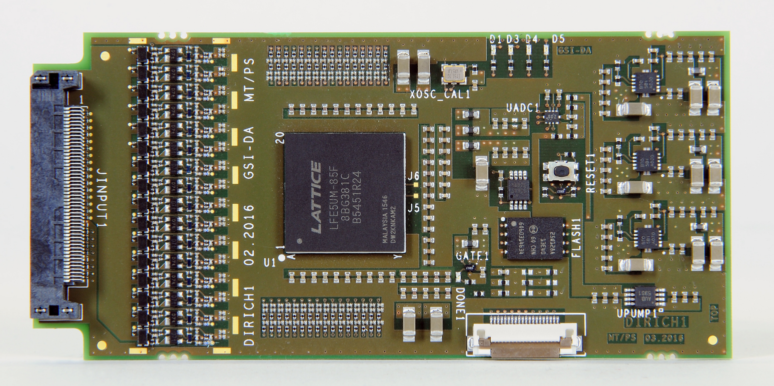
- FEE module for 32 channels
- Amplification, Discrimination, TDC + DAQ
- no signal cables
- analog input signals and digital output signals (serial transmission) over the same connector
- low power consumption
- only possible with newest FPGAs (price/performance) and very high pin-count connectors
- galvanically isolate PMT from FEE with transformers
  - reduces issues with HV-Power-Supply GND connection

DiRICH: Amplifier Schematics



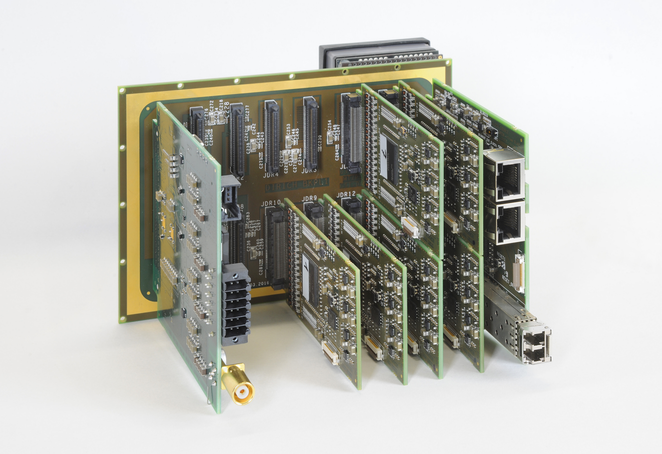
- BFU760F: fast transistor (40 GHz transition freq.)
- low power consumption: <9mW in simulation, 12mW in reality
- high gain: ~30
- simple (no specific higher order shaping)

DiRICH: In Real Life



- 47mm x 100mm area, 300μm x 600μm components, 0201 (imperial)
- transformer, gain 30 amps, 16bit-DAC, discriminator, high precision TDC, DAQ + TrbNet (2Gbit/s SERDES), slow-control and voltage-regulation

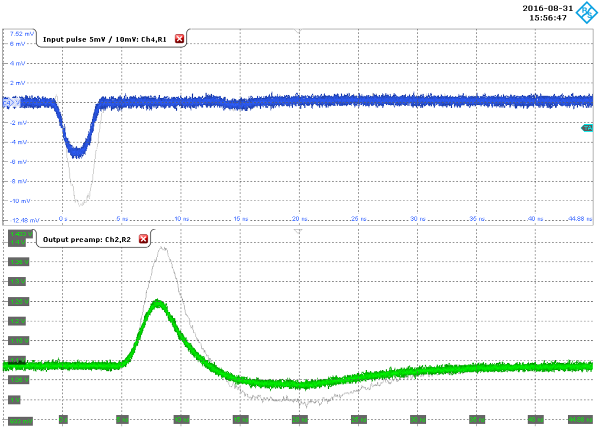
DiRICH: System



- DiRICH photos by Gabi Otto @GSI

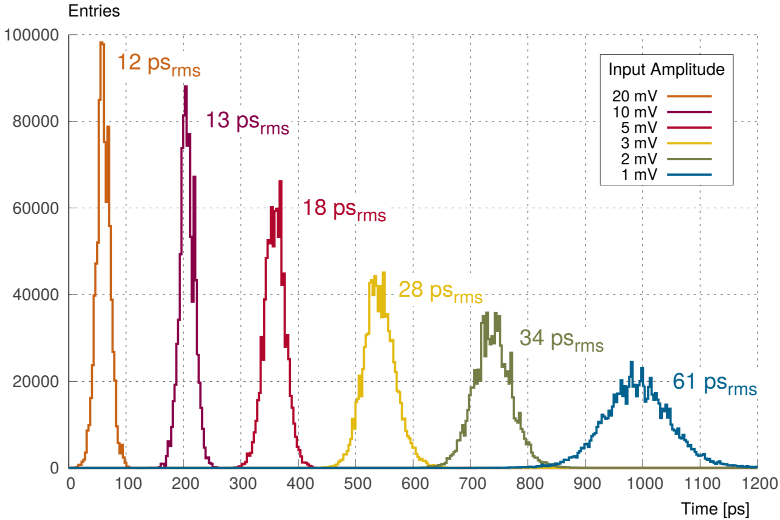
- Backplane for 6 PMTs (384 channels), 12 DiRICH and a data concentrator board and a power board.

Amplifier Results



- very good agreement to simulation
- Power: 12mW instead of 9mW

Time Precision measured with Input from Signal Generator



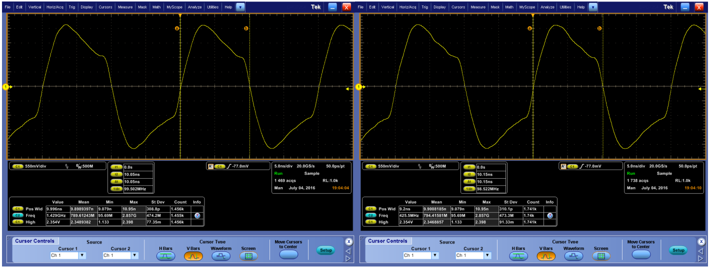
- measured with two signals to PMT-simulator (attenuator-PCB)

Issues with the Electronics (What took you so long?)

- Implementation of 8 channel TDC: very fast
- 32-channel TDC took quite some time to convince the FPGA-software to do it right (not made for such applications)
- many details need a lot of attention, discussion with the FPGA-vendor, time to understand, respin of new PCBs/assembly
- system tests need a large team working together (without beam :-))

Issues I: Smart and Modern FPGAs: PVT

- FPGAs are supposed to be stable from -40°C up to >80°C (made for automotive industry)
- "Process-Voltage-Temperature Compensation" of the drivers mentioned exactly once in the datasheet without any detail. Was unknown feature even for experts.



- PVT solution: Add two small simpler FPGAs to the DiRICH which just perform the DAC (temperature compensated) functionality

Issues II: ECP5 SERDES issues

Specs of Lattice ECP5

- 4 SERDES channels
- Up to 5 Gb/s (ECP5-5G) or 3.2Gb/s (ECP5)
- 17 application notes + datasheet
- SERDES application note: 100 pages
- 300 registers to configure

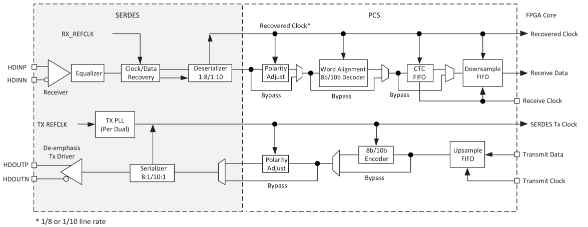


Figure 2.28. Simplified Channel Block Diagram for SERDES/PCS Block

Issues II: ECP5 SERDES issues

Operation of larger systems at nominal voltage

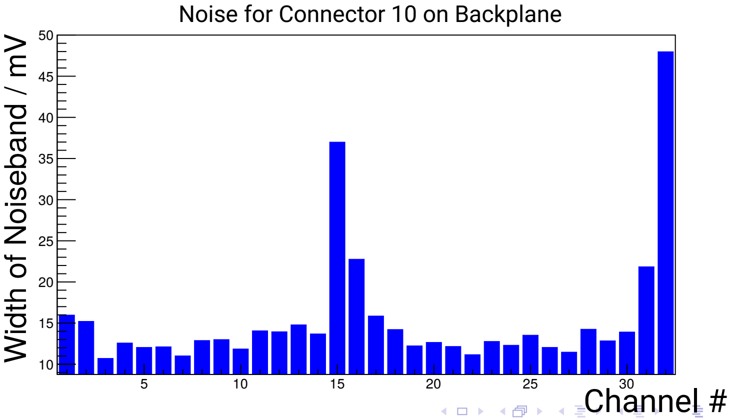
- for normal parameters ($\pm$1500ppm for loss of lock)
  - 1/3 of 30 DiRICH were working
- with more tolerance ($\pm$7000ppm)
  - 2/3 of the DiRICH were working
- with additional reduced voltage of Vcc (nominal 1.1V)
  - 4/5 of the DiRICH were working
  - done measurement with this, but unstable system
- Checking all details of schematics, datasheet, application notes, layout and at the end measure all inputs and outputs and long discussions with Lattice

Issues II: ECP5 SERDES issues, SERDES Supply

- After quite some struggling and systematic search
- SERDES needs 6 separate voltages
  - Vcc, VccHRX and VccHTX, VccA, VccAux, VccAuxA
  - default: all to 1.1V or 2.5V
- All supply voltages are "immune" to small changes (+-100mV)
- except VccA, for the PLL of the SERDES
- Operating from 0.90V to 1.04V
  - all fine!
  - Above ~1.06V PLL lock is lost
  - side note: for higher frequencies it works better
- Fix: Pi-Filter Ferrite Bead: BLM15- instead of BLM18-
  - series resistance: 1.1Ohm instead of 0.3Ohm
    - results in 70mV drop
- New iteration for DiRICH module with LDO for this voltage

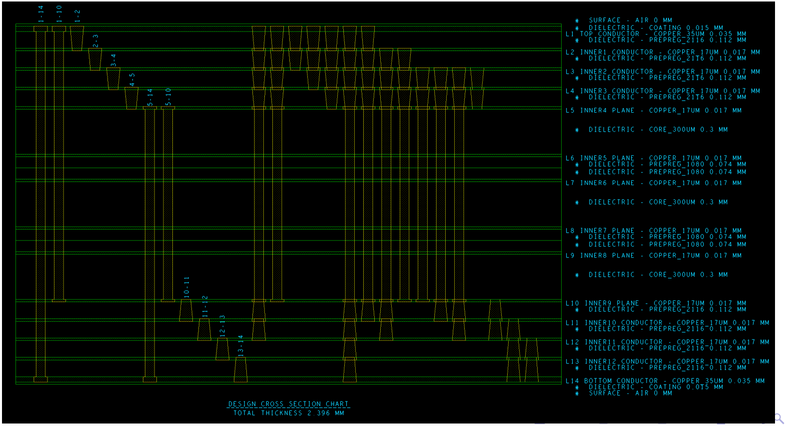
Issues III: Noise from Backplane

- Backplane: real challenge for the layout: EM isolate digital signals from analog ones while connectors overlap
- Observation: High noise for certain channels from the backplane



Issues III: Noise from Backplane, Backplane Layout

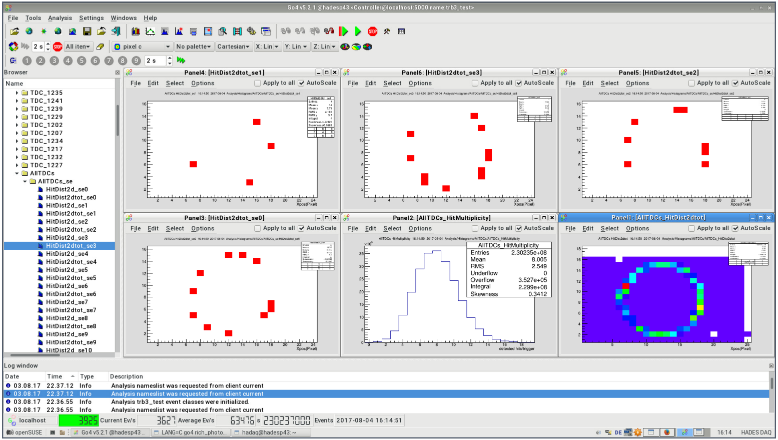
- isolation was not perfect at certain points where buried vias perforated the isolating GND-plane
- new improved backplane with 4 layers of stacked microvias (limit), 14 layers



Summary

- The TRB (with its associated FPGA-TDC + DAQ) is a mature platform (hardware and software) useful for many applications
  - Collaboration takes care of constant development and maintenance
- based on the "come-and-kiss" principle
  - no hard to acquire ASICs used
  - due to modern commercial components (small, less power) now closer to the ASIC domain
- limitations for larger systems
  - cable-hell and noise
- larger application specific systems: need to optimize
  - hard and software is "easy" to adapt to special applications
- MA-PMT and MCP-PMT applications are quite common and we can share the achievements and effort

Thank You for Your Attention



- Online display of MA-PMT signals from pulsed laser-photons. MA-PMT covered by a ring-mask. Single events and an integral are displayed. Data analysis without ToT-cut.